Application No. 10/706,457

IN THE CLAIMS:

1. (Currently Amended) A ~~semiconductor~~ substrate for a micro-fluid ejecting device, the substrate comprising:

   a plurality of fluid ejection devices ~~disposed on the substrate~~;

   a plurality of driver devices ~~transistors disposed on the substrate~~ for driving the plurality of fluid ejection devices; and

   a nonvolatile programmable memory matrix containing embedded programmable memory devices, the matrix being capable of being operatively connected to the micro-fluid ejecting device for ~~collecting and~~ storing information ~~on the semiconductor substrate~~ for operation of the micro-fluid ejecting device.

2. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the embedded programmable memory devices comprise transistors selected from the group consisting of PMOS and NMOS floating gate transistors.

3. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the embedded programmable memory devices have a memory density of greater than about 200 bits per square millimeter.

4. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the programmable memory matrix comprises floating gate transistors.

5. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the programmable memory matrix comprises more than 128 memory devices.

6. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the embedded programmable memory devices are programmable by applying a voltage of greater than about 8 volts for at least about 100 microseconds.

7. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the embedded programmable memory devices will pass from about 10 to about 200 microamps of

current at about 2 volts in a programmed state.

8. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the embedded programmable memory devices will pass less than 3 microamps of current at about 2 volts in an unprogrammed state.

9. (Currently Amended) The ~~semiconductor~~ substrate of claim 1 wherein the memory matrix is erasable by ultraviolet light and further comprising a layer disposed adjacent the programmable memory matrix, said layer having properties sufficient to block ultraviolet light having a wavelength below about 400 nanometers.

10. (Original)A printhead for an ink jet printer containing the semiconductor substrate of claim 9.

11. (Original) The printhead of claim 10 wherein the layer comprises a material selected from the group consisting of a photoresist material, and a metal layer, said layer having ultraviolet light blocking properties.

12. (Original) The printhead of claim 10 wherein the layer comprises a polyimide nozzle plate.

13. (Currently Amended) An ink jet printer cartridge for an ink jet printer comprising:
a cartridge body having an ink supply source and a printhead attached to the cartridge body in fluid communication with the ink supply source, the printhead comprising:
a ~~semiconductor~~ substrate having a plurality of ink ejection devices ~~disposed on the substrate~~;
a plurality of driver devices ~~transistors disposed on the substrate~~ for driving the plurality of ink ejection devices;
a nonvolatile programmable memory matrix containing embedded programmable memory devices, the matrix being operatively connected to the ink jet printer for ~~collecting and~~ storing

information ~~on the semiconductor substrate~~ for operation of the printer; and

a nozzle plate attached to the ~~semiconductor~~ substrate for ejecting ink therefrom upon activation of the ink ejection devices.

14. (Original) The ink jet printer cartridge of claim 13 wherein the embedded programmable memory devices comprise transistors selected from the group consisting of PMOS and NMOS floating gate transistors.

15. (Original) The ink jet printer cartridge of claim 13 wherein the embedded programmable memory devices have a memory density of greater than about 200 bits per square millimeter.

16. (Original) The ink jet printer cartridge of claim 13 wherein the programmable memory matrix comprises floating gate transistors.

17. (Original) The ink jet printer cartridge of claim 13 wherein the programmable memory matrix comprises more than 128 memory devices.

18. (Original) The ink jet printer cartridge of claim 13 wherein the embedded programmable memory devices are programmable by applying a voltage of greater than about 8 volts for at least about 100 microseconds.

19. (Original) The ink jet printer cartridge of claim 13 wherein the embedded programmable memory devices will pass from about 10 to about 200 microamps of current at about 2 volts in a programmed state.

20. (Original) The ink jet printer cartridge of claim 13 wherein the embedded programmable memory devices will pass less than 3 microamps of current at about 2 volts in an unprogrammed state.

21. (Currently Amended) The ink jet printer cartridge of claim 13 <u>wherein the memory matrix is erasable by ultraviolet light and</u> further comprising a photoresist layer disposed

adjacent the programmable memory matrix, said photoresist layer having properties sufficient to block ultraviolet light having a wavelength below about 400 nanometers.

22. (Currently Amended) The ink jet printer cartridge of claim 13 wherein the memory matrix is erasable by ultraviolet light and the nozzle plate comprises a polyimide nozzle plate having properties sufficient to block ultraviolet light having a wavelength below about 400 nanometers.

23. (New) A printhead for a micro-fluid ejecting device, the printhead comprising:

a plurality of fluid ejection devices;

a plurality of driver devices for driving the plurality of fluid ejection devices; and

a nonvolatile programmable memory matrix containing embedded programmable memory devices, the matrix being capable of being operatively connected to a micro-fluid ejecting device for storing information for operation of the micro-fluid ejecting device.

24. (New) The printhead of claim 23, further comprising a controller wherein at least a portion of the matrix is readable by the controller.

25. (New) The printhead of claim 24, further comprising a controller wherein the at least a portion of the matrix is directly readable by the controller.

26. (New) The printhead of claim 23, wherein the programmable memory devices are embedded in a semiconductor.

27. (New) The printhead of claim 26, wherein the semiconductor comprises silicon.

28. (New) The printhead of claim 23, wherein the driver devices comprise transistors.